Confirmation No. 4536

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	VENEZIA *et al.*	Examiner:	Tsai, H.
Serial No.:	10/539,224	Group Art Unit:	2895
Filed:	June 16, 2005	Docket No.:	BE020043 US1
Title:	METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE OBTAINED WITH SUCH A METHOD		

APPEAL BRIEF

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Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed February 19, 2009 and in response to the rejections of claims 1-10 as set forth in the Final Office Action dated October 20, 2008.

Please charge Deposit Account number 50-0996 (NXPS.273PA) $540.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 017439/0158 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-10 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Final Office Action dated October 20, 2008.

V. Summary of Claimed Subject Matter

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a method of manufacturing a semiconductor device (*see, e.g.*, device 10 shown in Figs. 1-6) with a semiconductor body of a semiconductor material (*see, e.g.*, body 1 shown in Figs. 1-6, and page 5:3-5), the semiconductor device including a field effect transistor having a source region and a drain region (*see, e.g.*, source and drain regions 2 and 3 shown in Fig. 3, and page 5:20-24) at a surface of the semiconductor body, and having a gate region (*see, e.g.*, gate 4 shown in Fig. 3) between the source region and the drain region, the gate region including a semiconductor region of a further semiconductor material (*see, e.g.*, polycrystalline region 4A shown in Fig. 3) that is separated from the surface of the semiconductor body by a gate dielectric (*see, e.g.*, gate oxide 5 shown in Fig. 3), the method comprising: forming the gate dielectric on the surface of the semiconductor body (*see, e.g.*,

page 5:13-19); forming the semiconductor region on the gate dielectric (*see, e.g.*, page 5:13-19); depositing a sacrificial region (*see, e.g.*, sacrificial region 4B shown in Fig. 3, and page 5:13-19) on top of the semiconductor region; after depositing the sacrificial region, forming spacers (*see, e.g.*, spacers 6 shown in Fig. 3, and page 5:24-30) adjacent to the gate region for forming the source and drain regions; forming the source and drain regions on the surface of the semiconductor body (*see, e.g.*, Fig. 3, and page 5:30-33); after forming the source and drain regions, selectively etching the sacrificial region with respect to the semiconductor region (*see, e.g.*, Fig. 4, and page 6:1-6); depositing a metal layer (*see, e.g.*, metal layer 7 shown in Fig. 4, and page 6:6-10) on the source region, the drain region, and the gate region; forming a compound (*see, e.g.*, region 8A shown Fig. 5, and page 6:11-20), that includes at least a portion of the source and drain regions, of the metal layer and the semiconductor material; and forming a compound (*see, e.g.*, region 8B shown Fig. 5, and page 6:11-20), that includes at least a substantial portion of the further semiconductor material, of the metal layer and the further semiconductor material.

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

VI. Grounds of Rejection to be Reviewed Upon Appeal

The grounds of rejection to be reviewed on appeal are as follows:

A. Claims 1-2 and 10 stand rejected under 35 U.S.C. § 102(b) over the Wang reference (U.S. Patent No. 6,074,922).

B. Claims 3-7 and 9 stand rejected under 35 U.S.C. § 103(a) over the Wang reference in view of the Hashimoto reference (U.S. Patent Pub. 2001/0003056).

C. Claim 8 stands rejected under 35 U.S.C. § 103(a) over the Wang reference in view of the Wu reference (U.S. Patent No. 6,348,390).

VII. Argument

Appellant's interpretation of the claim limitations precludes correspondence under by 35 U.S.C. § 102(b) in view of the '922 reference. The Examiner has not presented an alternative interpretation. The Examiner has not alleged fault with Appellant's interpretation. Thus, despite Appellant's facilitating amendments and reasoned arguments directed at these structural differences, the Examiner has not rebutted or addressed Appellant's interpretation. Any hypothetical interpretation put forth by the Examiner at this late stage would therefore be unsupported by the prosecution history and would represent new grounds for rejection. Due to this lack of alternatives and disputed facts, the record conclusively establishes structural differences between the teachings of the '922 reference and the claimed limitations. The rejection under 35 U.S.C. § 102(b) in view of the '922 reference is improper and should be reversed.

There is also insufficient evidence to sustain the rejections under 35 U.S.C. § 103(a). Appellant has shown that one of skill in the art would find no reason to modify the '922 reference in the manner proposed by the Examiner because the '922 reference teaches away from such modification and because the Examiner's asserted modification undermines the purpose and operation of the '922 reference. The Examiner chose not to respond to Appellant's arguments during prosecution. Only at the Advisory Action did the Examiner attempt a direct response to Appellant's arguments; however, the response of Advisory Action fails to address Appellant's arguments and shows a lack of understanding of the

proper standards for assessing rejections under 35 U.S.C. § 103(a). Thus, the rejections under 35 U.S.C. § 103(a) are improper for failing to properly consider factors and evidence of nonobviousness and for failing to apply the proper standard of review.

Procedurally, the Examiner's failure to respond is well documented. Regarding the rejection under 35 U.S.C. § 102(b), it is not disputed, and relatively easy to show with a side-by-side comparison, that the '922 reference has structural differences from Appellant's disclosed embodiments. To highlight these differences, Appellant introduced amendments, supported by reasoned arguments, which were directed at such structural differences, thereby precluding anticipation by the '922 reference. Despite several opportunities, the Examiner chose not to provide substantive evidence or reasoned explanations for maintaining the anticipation rejection in view of the '922 reference. *See* Office Action of April 8, 2008 (a restatement of rejections without direct explanation or response to Appellant's arguments); Office Action of October 20, 2008 (recitation of generic law without explanation as to the relevance of the generic law). The Examiner has not provided an alternate interpretation, nor has the Examiner provided reasoned explanations as to any fault in Appellant's interpretation. The interpretation put forth by Appellant is the only interpretation in the record. As Appellant's interpretation precludes anticipation by the '922 reference (as discussed in more detail hereafter), the record provides insufficient support to maintain the rejection. For the aforementioned reasons, Appellant requests that the Board reverse the rejections of all pending claims 1-10 because the '922 reference is deficient in that it does not teach or suggest all the elements of Appellant's claims, and in particular the claimed aspects related to forming a compound of a metal layer and semiconductor gate material, with the compound including at least a substantial portion of the gate material.

Regarding the rejection under 35 U.S.C. § 103(c), Appellant twice presented arguments regarding the impropriety of the Examiner's proposed modification of the '922 reference to which the Examiner chose not to respond with any reasoned explanation. It was not until Appellant presented these arguments a third time that the Examiner (in the Advisory Action dated January 28, 2009) attempted any substantive explanation for the rationale behind the proposed combination. The Examiner's response, however, shows a misunderstanding of both Appellant's argument and of the proper standard for assessing obviousness-type

rejections. In this latest response, the Examiner improperly concludes that because the alleged combination is asserted to be "within the level of the skill of the skilled person in the art" the combination is proper; however, whether or not the combination was within the level of the skilled artisan was not a disputed issue. Thus, the Examiner has not rebutted Appellant's showing of the impropriety of the rejection nor is such a statement sufficient to establish obviousness. There is no evidence of record that the Examiner has properly considered the evidence and arguments put forth by Appellant. If the combination was simply a "predictable" combination of teachings fitting together "like pieces of a puzzle" and only involving "ordinary common sense," the Examiner should have had little trouble rebutting Appellant's strong evidence of nonobviousness. Instead, the Examiner chose not to respond until the Advisory Action and then to only present a largely conclusory response that fails to rebut or show consideration of the necessary factors. As will be explained in more detail hereafter, the record shows by a preponderance of the evidence that the '922 reference teaches away from the proposed combination, which also undermines the purpose and operation of the '922 reference.

A. The Rejection Of Claims 1-2 And 10 Under U.S.C. § 102(b) Over The '922 Reference Should Be Reversed Because The '922 Reference Fails To Disclose That A Layer Of Semiconductor Gate Material Is Substantially Transformed Into Compound Of Semiconductor And Metal Material

To sustain a § 102 rejection, each and every claim element must be taught by the applied reference. Appellant submits that the '922 reference clearly fails to meet this standard because the '922 reference does not disclose forming a compound, that includes at least a substantial portion of the further semiconductor material (*i.e.,* the gate region), of the metal layer and the further semiconductor material. Rather, the '922 reference teaches that silicide 42 (*i.e.,* the asserted compound) is formed on top of polysilicon gate 16 (*i.e.,* the asserted further semiconductor material) from titanium layer 40 (*i.e.,* the asserted metal layer). *See, e.g.,* Figures 6-8.

Certain embodiments of Appellant's invention relate to improved manufacturing methods and devices created from the improved manufacturing methods. In particular,

manufacturing methods create a field effect transistor with a polysilicon gate. Appellant's device remains relatively planar thereby simplifying subsequent deposition, patterning and etching steps. Appellant's methods also do not require complex photolithography or CMP processes. The manufacturing methods include a series of steps, an important one of which involves the formation of a compound within a substantial portion of the semiconductor gate material and also within a portion of the source and drain regions. That is to say that a deposited layer of semiconductor gate material is substantially transformed into a compound of semiconductor and metal material. The gate section 4A is transformed to a compound (8B) as are portions (8A) of the source and drain sections 2A and 3A. *See, e.g.,* Figures 4 and 5 reproduced below for the convenience of the Board.

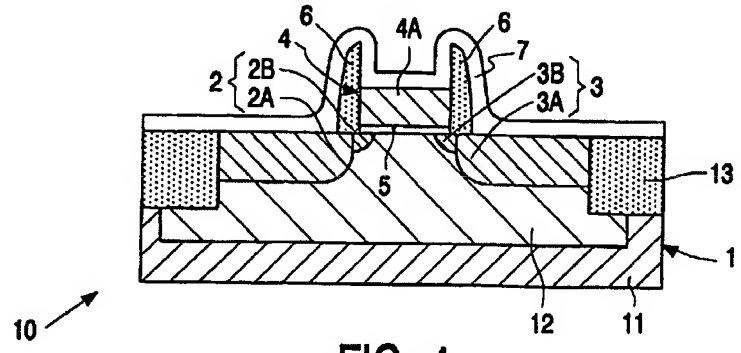

FIG. 4

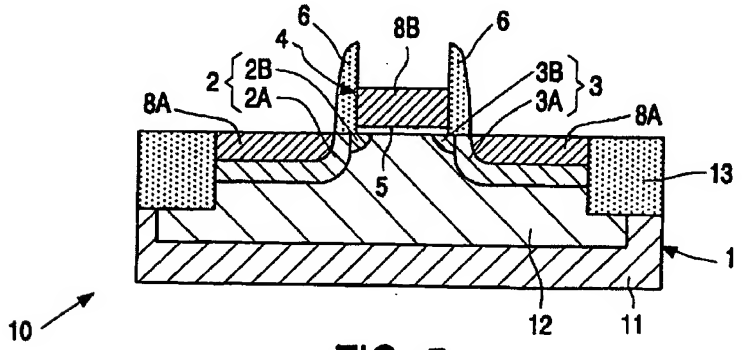

FIG. 5

The transformation of gate section 4A, and of parts of regions 2A and 3A, is accomplished, for example, by a specific two-part heating process.

Returning now to the cited prior art, the '922 reference does not teach or suggest transforming the gate, source and drain regions as in the claimed invention. Instead, the '922 reference seeks to transform metal region 40 located on top of the semiconductor gate 16 and also on top of the source and drain regions 36. *See, e.g.,* Figures 6 and 8 reproduced below for the convenience of the Board.

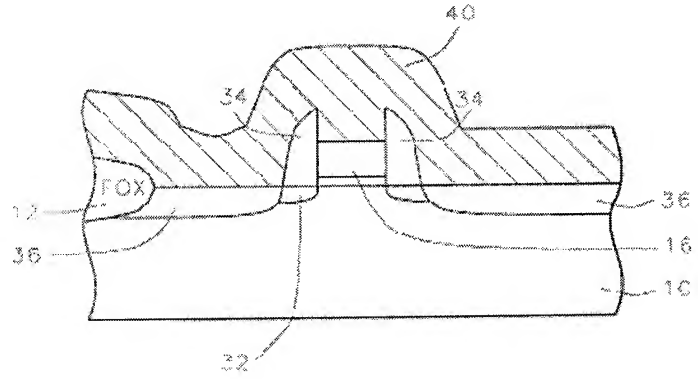

FIG. 6

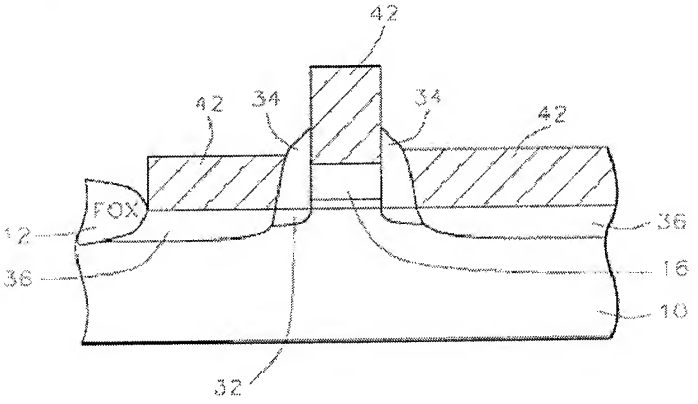

FIG. 8

Appellant submits that it should be readily apparent that section 42 of the '922 reference does not correspond to Appellant's sections 8A and 8B. When compared to Appellant's claimed invention and corresponding teachings, it has not been disputed that the '922 reference teaches a distinctly different device and goals as well as the use of different methods to accomplish these different goals. Appellant has introduced additional claim amendments to further clarify these differences; however, the Examiner has chosen not to explain these

differences other than reciting Figure 8, which has been shown to be clearly distinguishable from the claimed invention.

The only interpretation of the relevant claim terms is the interpretation put forth by Appellant. This interpretation precludes anticipation by the '922 reference because it requires that a substantial portion of the gate region be transformed into the compound. Appellant's interpretation finds support in the plain meaning of the terms, the logical explanations provided by Appellant and by Appellant's specification. Appellant has made repeated efforts to explain and clarify the differences between the claimed invention and the '922 reference, including arguments and clarifying and facilitating amendments. Despite Appellant's focus on these differences, the Examiner has never presented an alternative interpretation that would explain the rationale for maintaining the rejection. The record does not contain sufficient evidence to establish correspondence to each element of the claimed invention. Thus, the Examiner has failed to establish correspondence to the claimed invention, to present an alternate interpretation and to rebut Appellant's arguments. Appellant submits that the evidence of record weighs heavily in favor of Appellant and is more than sufficient to establish lack of correspondence by a preponderance of the evidence. For at least these reasons, Appellant submits that the § 102(b) rejection of claims 1-2 and 10 fails, and therefore requests reversal of the rejection.

B. The Rejections Of Claims 3-7 And 9 Under U.S.C. § 103(a) Over The '922 Reference In View Of The '056 Reference Should Be Reversed Because There Is No Motivation For The Skilled Artisan To Modify The '922 Reference In The Manner Proposed By Examiner

The Examiner's asserted modifications of the '922 reference undermine the purpose and operation of the '922 reference.

1. The Rejection Of Claim 3 Under U.S.C. § 103(a) Over The '922 Reference In View Of The '056 Reference Should Be Reversed Because There Is No Motivation For The Skilled Artisan To Modify The '922 Reference In The Manner Proposed By Examiner

Appellant's claim 3 sets forth that the "further semiconductor region is completely consumed during the formation of the compound of the metal layer and the further semiconductor material." In contrast, the '922 reference transforms the titanium layer 40 into titanium silicide 42 while avoiding transformation or consumption of its gate electrode 16. *See, e.g.,* Figures 6-7 and Col. Col. 3:59 to Col. 4:15. Apparently recognizing this issue, the Examiner proposes that the prior art would lead a skilled artisan to modify the teaching of the '922 reference by the '056 reference's teaching that, for a certain embodiment in the '056 reference, the'056 reference's gate can be consumed as part of its semiconductor manufacturing process.

Appellant disagrees and submits that the skilled artisan would not be motivated to implement such a modification of the '922 reference in part because the modification attempts to solve a problem that is not present in the cited embodiment and because the modification drastically alters the entire process and structure taught by the '922 reference. In this and other regards, the '922 reference clearly teaches away from this modification proposed by the Office Action. *See, e.g.,* M.P.E.P. § 2145. In *KSR,* the Supreme Court looked favorably on *Adam's* treatment of teaching away stating, "when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious." *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007). As is well-established (before and after the KSR decision), such a rejection is improper because the proposed modification would undermine the main objective and embodiment of the '922 reference and/or is based on an attempt to solve a problem that is not present in (and not needing to be addressed by) the '922 reference.

Moreover, a main objective of the '922 reference is to form a metal silicide on the top surface of the gate electrode in order to solve the resistance degradation problem for narrow polysilicon lines caused by salicide non-uniformity (discussed in the background section of the '922 reference and at Col. 4:12-14) and to *increase* the polysilicon width. "The process

of the invention provides an effective method of fabricating an integrated circuit device having a silicided polysilicon gate with reduced resistance, increased effective polysilicon width, increased salicide thickness, improved yield, and reduced gate to source/drain bridging." '922 reference, Col. 5:33-37 (emphasis added). Nevertheless, the Examiner proposes completely removing the polysilicon of the gate electrode. The skilled artisan would understand that various steps taught by the '922 reference are implemented for the reasons taught by the '922 reference. Logic dictates that the steps of the primary reference would not be obvious to implement only to then undo the very reasons for why the skilled artisan would seek to perform the original steps. Rather than producing a device having an increased salicide thickness and effective polysilicon thickness (*see, e.g.*, '922 reference, Abstract), the proposed modification completely removes the polysilicon. Accordingly, the rejection violates M.P.E.P. § 2143.01. *See also In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984) (A §103 rejection cannot be maintained when the asserted modification undermines the purpose of the main reference).

Modifying the '922 reference in the manner proposed by the Examiner (*i.e.*, such that gate electrode 16 is completely consumed) is further improper because it changes the principal operation of the '922 reference. *See, e.g.*, M.P.E.P. § 2143.01 ("If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)"). Were the gate of the '922 reference to be completely consumed, it would change the principal operation of the '922 reference, *e.g.*, by eliminating the polysilicon thickness.

In view of the above, there is no motivation for the skilled artisan to modify the '922 reference in the manner proposed by the Examiner. Accordingly, the § 103(a) rejection of claim 3 is improper and Appellant requests that it be reversed.

2. The Rejection Of Claims 4-7 And 9 Under U.S.C. § 103(a) Over The '922 Reference In View Of The '056 Reference Should Be Reversed Because There Is No Motivation For The Skilled Artisan To Modify The '922 Reference In The Manner Proposed By The Examiner

The Examiner's proposed modification of the '922 reference to use the two step heating process of the '056 reference undermines the purpose and operation of the '922 reference. *See, e.g.,* M.P.E.P. § 2143.01 and also *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984) (A §103 rejection cannot be maintained when the asserted modification undermines the purpose of the main reference). In this instance, a main objective of the '922 reference is to reduce bridging between the gate and the source/drain. For example, the '922 reference states "The process of the invention provides an effective method of fabricating an integrated circuit device having a silicided polysilicon gate with reduced resistance, increased effective polysilicon width, increased salicide thickness, improved yield, and reduced gate to source/drain bridging." '922 reference, Col. 5:33-37 (emphasis added). Appellant submits that the Examiner's proposed combination would result in the gate being shorted to the source/drain thereby undermining the purpose of the '922 reference.

The Examiner's alleged reason to combine the '922 and '056 reference is so that "agglomeration is less likely to occur at the surface" of the CoSi layer as taught in paragraph 0097 of the '056 reference. The '056 reference further teaches that these alleged benefits result from depositing a silicon film on the surface of the device in between the first and second heat treatments. *See, e.g.,* paragraph 0096. As such, the Examiner's proposed combination would necessarily result in an additional layer of silicon being deposited on the device of the '922 reference after the first heating step. For convenience, Appellant has reproduced Fig. 7 of the '922 reference. Fig. 7 illustrates the device of the '922 reference after the first heating step. Appellant has modified the figure to show the additional silicon layer taught to be necessary for obtaining the alleged advantage of reduced agglomeration.

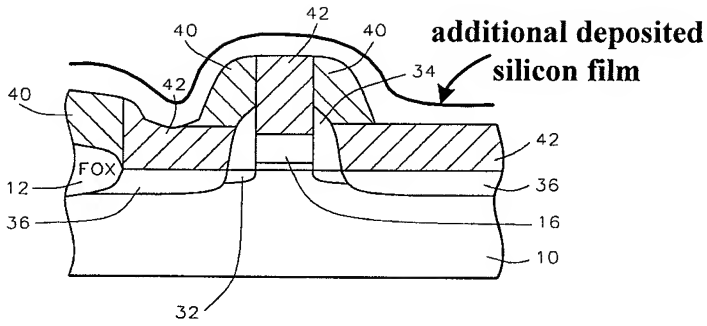

FIG. 7

Appellant submits that then applying the second heating step to the device shown above in Fig. 7 would result in the unreacted titanium 40 being transformed into titanium silicide, which would cause the gate 16 to be shorted to the source and drain regions 36. As such, the addition of the two step heating process of the '056 reference to the '922 reference would defeat the '922 reference's purpose of reducing bridging between the gate and the source/drain and render the device inoperable.

In view of the above, there is no motivation for the skilled artisan to modify the '922 reference in the manner proposed by the Examiner. Accordingly, the § 103(a) rejection of claims 4-7 and 9 is improper and Appellant requests that it be reversed.

C. The Rejection Of Claim 8 Under U.S.C. § 103(a) Over The '922 Reference In View Of The '390 Reference Should Be Reversed Because No Valid Reason Has Been Presented To Modify The '922 Reference

The § 103(a) rejection of claim 8 is improperly based on hindsight without taking into consideration that the '922 reference already adequately addresses the identified problem without the Examiner's proposed modifications. Without a valid reason to modify the '922 reference with the cited teachings of the '390 reference, the rejection fails to meet the requirements of § 103 and relevant law. *See, e.g., KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007) ("A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art."). The recent Supreme Court decision in *KSR Int'l Co. v. Teleflex Inc* has clarified that there must be a valid reason to combine the references, and numerous USPTO Appeals Board decisions have cited this case as support for overturning Examiners' rejections for lacking of adequate rationale to combine. Because no valid reason to modify has been presented, Appellant requests that the Board reverse the § 103(a) rejection of claim 8.

In regard to claim 8, the Examiner acknowledges that the'922 reference does not teach removing spacers 34. The Examiner then asserts that the skilled artisan would modify the'922 reference to remove the spacers 34 as taught by the '390 reference in order "to form extended source/drain regions." The '922 reference, however, already teaches that lightly doped source and drain regions 32 (*i.e.,* extended source/drain regions) are formed prior to the formation of the spacers 34. *See, e.g.,* Figures 2-4 and Col. 3:35-36. Appellant submits that the Examiner's alleged motivation for the proposed combination is based on a nonexistent problem that has already been addressed by the '922 reference. Accordingly, the Examiner has not provided any evidence as to why one of skill in the art would find the asserted combination obvious as required.

In view of the above, the § 103(a) rejection of claim 8 is improper and Appellant requests that it be withdrawn.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-10 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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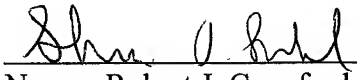
By: 

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/539,224)

1. A method of manufacturing a semiconductor device with a semiconductor body of a semiconductor material, the semiconductor device including a field effect transistor having a source region and a drain region at a surface of the semiconductor body, and having a gate region between the source region and the drain region, the gate region including a semiconductor region of a further semiconductor material that is separated from the surface of the semiconductor body by a gate dielectric, the method comprising:

forming the gate dielectric on the surface of the semiconductor body;

forming the semiconductor region on the gate dielectric;

depositing a sacrificial region on top of the semiconductor region;

after depositing the sacrificial region, forming spacers adjacent to the gate region for forming the source and drain regions;

forming the source and drain regions on the surface of the semiconductor body;

after forming the source and drain regions, selectively etching the sacrificial region with respect to the semiconductor region;

depositing a metal layer on the source region, the drain region, and the gate region;

forming a compound, that includes at least a portion of the source and drain regions, of the metal layer and the semiconductor material; and

forming a compound, that includes at least a substantial portion of the further semiconductor material, of the metal layer and the further semiconductor material.

2. A method as claimed in claim 1, characterized in that the spacers are formed by depositing a layer of a dielectric material on top of the semiconductor body on which the gate region comprising the semiconductor region and the sacrificial region is present and by subsequently removing the deposited layer on top of and on both sides of the gate region by etching.

3. A method as claimed in claim 1, characterized in that the further semiconductor region is completely consumed during the formation of the compound of the metal layer and the further semiconductor material.

4. A method as claimed in claim 1, characterized in that the formation of the compounds between the metal and the semiconductor material and the metal and the further semiconductor material is carried out in two separate heating steps,

the first heating step resulting in an intermediate compound with a low content of the semiconductor material or of the further semiconductor material and in

the second heating step the intermediate compound being converted to the compound having a higher content of the semiconductor material or of the further semiconductor material.

5. A method as claimed in claim 4, characterized in that between the two heating steps, a part of the metal layer which has not reacted to form the intermediate compound is removed by etching.

6. A method as claimed in claim 4, characterized in that between the two heating steps, a layer of the further semiconductor material is deposited on the surface of the semiconductor body.

7. A method as claimed in claim 6, characterized in that after the second heating step, a part of the layer of the further semiconductor material which has not reacted to form the compound is removed by etching.

8. A method as claimed in claim 1, characterized in that after the formation of the compounds of the metal and the semiconductor material and of the metal and the further semiconductor material, the spacers are removed.

9. A method as claimed in claim 4, characterized in that for the semiconductor material as well as for the further semiconductor material silicon is chosen, and for the intermediate compound and for the compound of the metal and the semiconductor material and the further semiconductor material a metal silicide is chosen.

10. A semiconductor device comprising a field effect transistor obtained by a method as claimed in anyone of the preceding claims.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.